AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A control system to control an output regulator, the output regulator to convert an input voltage to a regulated output, the output regulator including a power stage to generate a power output from the input voltage and an output filter to filter the power output to generate the regulated output, the control system comprising:

a digital controller, responsive to a sense signal corresponding to the regulated output, to generate a drive signal to control the power stage, the digital controller including and selecting between at least three operating modes, a selected one of the operating modes to generate the drive signal, wherein said digital controller switches from each of said at least three operating modes to remaining ones of said at least three operating modes based on said sense signal.

2. (Original) The control system of Claim 1 further including a clock to generate a clock signal having clock cycles; and

wherein the digital controller selects, in synchrony with the clock signal, the one of the at least three operating modes.

3. (Original) The control system of Claim 2 wherein the digital controller switches between the at least three operating modes on a clock cycle by clock cycle

basis.

4. (Original) The control system of Claim 1 further comprising an output sensor to generate the sense signal.

5. (Original) The control system of Claim 4 wherein the output sensor is selected from the group consisting of voltage sensors, current sensors, and phase sensors.

6. (Original) The control system of Claim 1 wherein the at least three operating modes include hysteretic modes, adaptive hysteretic modes, pulse width modulated modes, constant on-time modes, constant off-time modes, resonant modes, fixed frequency soft-switching modes, voltage modes, current modes, fixed frequency modes, variable frequency modes, and combinations thereof.

7. (Original) The control system of Claim 1 wherein the digital controller further generates a duty cycle estimation for controlling the power stage.

8. (Original) The control system of Claim 7 further comprising a delay line to adjust the duty cycle estimation.

9. (Original) The control system of Claim 1 wherein the digital controller has a switching mode selected from a group consisting of synchronous switching,

asynchronous switching, and multi-frequency switching.

10. (Original) The control system of Claim 1 wherein the sense signal represents a difference between a reference and the regulated output.

11. (Original) The control system of Claim 10 wherein the reference is selected from a group consisting of reference voltages and reference currents.

12. (Original) The control system of Claim 1 wherein the regulated output is selected from the group comprising output voltage, output current, and output power.

13. (Original) The control system of Claim 1 further comprising an output selector to set a nominal value of the regulated output.

14. (Original) The control system of Claim 13 wherein the output selector generates a reference signal in response to an input, the reference signal to set the nominal value of the regulated output.

15. (Currently Amended) A method of controlling a regulated output of an output regulator, comprising:

generating a sense signal corresponding to the regulated output;

providing at least three operating modes for generating a drive signal;

evaluating the sense signal;

selecting one of the at least three operating modes based the evaluating the sense signal, wherein switching from each of said at least three operating modes to remaining ones of said at least three operating modes is based on said sense signal; and

generating the drive signal as a function of the selected operating mode and in response to the sense signal to control the power stage.

16. (Original) The method of Claim 15 further including generating a clock signal having clock cycles; and

wherein the selecting one of the at least three operating modes is in synchrony with the clock signal.

17. (Original) The method of Claim 16 further including switching between the at least three operating modes on a clock cycle by clock cycle basis.

18. (Original) The method of Claim 15 wherein an output sensor generates the sense signal.

19. (Original) The method of Claim 18 wherein the output sensor is selected from the group *consisting* of voltage sensors, current sensors, and phase sensors.

20. (Original) The method of Claim 15 wherein the at least three operating modes include hysteretic modes, adaptive hysteretic modes, pulse width modulated

modes, constant on-time modes, constant off-time modes, resonant modes, fixed frequency soft-switching modes, voltage modes, current modes, fixed frequency modes, variable frequency modes, and combinations thereof.

21. (Original) The method of Claim 15 wherein generating the drive signal further includes generating a duty cycle estimation for controlling the generating of the power output.

22. (Original) The method of Claim 21 wherein generating the duty cycle estimation further includes generating an incremental delay to adjust the duty cycle esimation.

23. (Original) The method of Claim 15 further comprising a switching mode selected from a group consisting of synchronous switching, asynchronous switching, and multi-frequency switching.

24. (Original) The method of Claim 15 wherein generating the sense signal includes determining a difference between a reference and the regulated output.

25. (Original) The method of Claim 24 wherein the reference is selected from a group consisting of reference voltages and reference currents.

26. (Original) The method of Claim 15 wherein the regulated output is

selected from the group comprising output voltage, output current, and output power.

27. (Original) The method of Claim 15 further comprising setting a nominal value of the regulated output.

28. (Original) The method of Claim 27 wherein setting the nominal value further includes generating a reference signal in response to an input, the reference signal to set the nominal value of the regulated output.

29. (Currently Amended) A control system to control an output regulator, the output regulator to convert an input voltage to a regulated output, the output regulator including a power stage to generate a power output from the input voltage and an output filter to filter the power output to generate the regulated output, the control system comprising:

digital controller means, responsive to a sense signal corresponding to the regulated output, to generate a drive signal to control the power stage, the digital controller means including and selecting between at least three operating modes, a selected one of the operating modes to generate the drive signal, wherein said digital controller means switches from each of said at least three operating modes to remaining ones of said at least three operating modes based on said sense signal.

30. (Original) The control system of Claim 29 further including means for generating a clock signal having clock cycles; and

wherein the digital controller means selects one of the at least three operating modes in synchrony with the clock signal.

31. (Original) The control system of Claim 30 the digital controller means switches between the at least three operating modes on a clock cycle by clock cycle basis.

32. (Original) The control system of Claim 30 wherein a means for output sensing generates the sense signal.

33. (Original) The control system of Claim 32 wherein the output sensing means is selected from the group consisting of voltage sensors, current sensors, and phase sensors.

34. (Original) The control system of Claim 29 wherein the at least three operating modes include hysteretic modes, adaptive hysteretic modes, pulse width modulated modes, constant on-time modes, constant off-time modes, resonant modes, fixed frequency soft-switching modes, voltage modes, current modes, fixed frequency modes, variable frequency modes, and combinations thereof.

35. (Original) The control system of Claim 29 wherein the digital controller means further to generate a duty cycle estimation for controlling the power stage.

36. (Original) The control system of Claim 35 further includes means for generating an incremental delay to adjust the duty cycle estimation.

37. (Original) The control system of Claim 29 further comprising a switching mode selected from a group consisting of synchronous switching, asynchronous switching, and multi-frequency switching.

38. (Original) The control system of Claim 29 wherein the sense signal represents a difference between a reference and the regulated output.

39. (Original) The control system of Claim 38 wherein the reference is selected from a group consisting of reference voltages and reference currents.

40. (Original) The control system of Claim 29 wherein the regulated output is selected from the group comprising output voltage, output current, and output power.

41. (Original) The control system of Claim 29 further comprising means for output selecting to set a nominal value of the regulated output.

42. (Original) The control system of Claim 41 wherein the means for output selecting to generate a reference signal in response to an input, the reference signal to set the nominal value of the regulated output.

43. (Currently Amended) An output regulator to convert an input voltage to a regulated output, comprising:

a power stage to generate a power output from the input voltage;

an output filter to filter the power output to generate the regulated output;

an output sensor to generate a sense signal corresponding to the regulated output; and

a digital controller, responsive to the sense signal, to generate a drive signal to control the power stage, the digital controller including and selecting between at least three operating modes, a selected one of the operating modes to generate the drive signal to control the power stage, wherein said digital controller switches from each of said at least three operating modes to remaining ones of said at least three operating modes based on said sense signal.

44. (Original) The output regulator of Claim 43 wherein the power stage has a configuration selected from the group consisting of linear regulators and switching regulators.

45. (Original) The output regulator of Claim 44 wherein the power stage of the switching regulator is a topology selected from the group consisting of buck, boost, Cuk, zeta, buck-boost, and sepic.

46. (Original) The output regulator of Claim 43 wherein the output sensor is

selected from a group consisting of voltage sensors, current sensors, and power sensors.

47. (Original) The output regulator of Claim 43 further including a clock to generate a clock signal having clock cycles; and

wherein the digital controller selects, in synchrony with the clock signal, the one of the at least three operating modes.

48. (Original) The output regulator of Claim 47 wherein the digital controller switches between the at least three operating modes on a clock cycle by clock cycle basis.

49. (Original) The output regulator of Claim 43 wherein the at least three operating modes include hysteretic modes, adaptive hysteretic modes, pulse width modulated modes, constant on-time modes, constant off-time modes, resonant modes, fixed frequency soft-switching modes, voltage modes, current modes, fixed frequency modes, variable frequency modes, and combinations thereof.

50. (Original) The output regulator of Claim 43 wherein the digital controller further generates a duty cycle estimation for controlling the power stage.

51. (Original) The output regulator of Claim 50 further comprising a delay line to adjust the duty cycle estimation.

52. (Original) The output regulator of Claim 43 wherein the digital controller has a switching mode selected from a group consisting of synchronous switching, asynchronous switching, and multi-frequency switching.

53. (Original) The output regulator of Claim 43 wherein the sense signal represents a difference between a reference and the regulated output.

54. (Original) The output regulator of Claim 53 wherein the reference is selected from a group consisting of reference voltages and reference currents.

55. (Original) The output regulator of Claim 43 wherein the regulated output is selected from the group comprising output voltage and output current.

56. (Original) The output regulator of Claim 43 further comprising an output selector to set a nominal value of the regulated output.

57. (Original) The output regulator of Claim 56 wherein the output selector generates a reference signal in response to an input, the reference signal to set the nominal value of the regulated output.

58. (Currently Amended) A method of generating a regulated output from an input voltage, comprising:

generating a power output from the input voltage; filtering the power output to generate the regulated output;

generating a sense signal corresponding to the regulated output;

providing at least three operating modes for generating a drive signal;

evaluating the sense signal;

selecting one of the at least three operating modes based the evaluating the sense signal, wherein switching from each of said at least three operating modes to remaining ones of said at least three operating modes is based on said sense signal; and

generating the drive signal as a function of the selected operating mode and in response to the sense signal to control the power stage.

59. (Original) The method of Claim 58 wherein the power stage has a configuration selected from the group consisting of linear regulators and switching regulators.

60. (Original) The method of Claim 59 wherein the power stage of the switching regulator is a topology selected from the group consisting of buck, boost, Cuk, zeta, buck-boost, and sepic.

61. (Original) The method of Claim 58 wherein generating the sense signal is selected from a group consisting of voltage sensor sensing, current sensor sensing, and power sensor sensing.

62. (Original) The method of Claim 58 further including generating a clock signal having clock cycles; and

wherein the selecting one of the at least three operating modes is in synchrony with the clock signal.

63. (Original) The method of Claim 62 further including switching between the at least three operating modes on a clock cycle by clock cycle basis.

64. (Original) The method of Claim 59 wherein the at least three operating modes include hysteretic modes, adaptive hysteretic modes, pulse width modulated modes, constant on-time modes, constant off-time modes, resonant modes, fixed frequency soft-switching modes, voltage modes, current modes, fixed frequency modes, variable frequency modes, and combinations thereof.

65. (Original) The method of Claim 63 wherein the generating the drive signal further includes generating a duty cycle estimation for controlling the generating of the power output.

66. (Original) The method of Claim 65 wherein generating the duty cycle estimation further includes generating an incremental delay to adjust the duty cycle estimation.

67. (Original) The method of Claim 58 further comprising a switching mode selected from a group consisting of synchronous switching, asynchronous switching, and multi-frequency switching.

68. (Original) The method of Claim 58 wherein generating the sense signal includes determining a difference between a reference and the regulated output.

69. (Original) The method of Claim 68 wherein the reference is selected from a group consisting of reference voltages and reference currents.

70. (Original) The method of Claim 58 wherein the regulated output is selected from the group comprising output voltage, output current, and output power.

71. (Original) The method of Claim 58 further comprising setting a nominal value of the regulated output.

72. (Original) The method of Claim 71 wherein setting the nominal value further includes generating a reference signal in response to an input, the reference signal to set the nominal value of the regulated output.

73. (Currently Amended) An output regulator to convert an input voltage to a regulated output, comprising:

means for generating a power output from the input voltage;

means for filtering the power output to generate the regulated output;

means for generating a sense signal corresponding to the regulated output;

digital controller means, responsive to the sense signal, to generate a drive signal to control the power stage, the digital controller means including and selecting between at least three operating modes, a selected one of the operating modes to generate the drive signal to control the power stage, wherein said digital controller means switches from each of said at least three operating modes to remaining ones of said at least three operating modes based on said sense signal.

74. (Original) The output regulator of Claim 73 wherein the means for generating the power output has a configuration selected from the group consisting of linear regulators and switching regulators.

75. (Original) The output regulator of Claim 74 wherein the means for generating the power output is a topology selected from the group consisting of buck, boost, Cuk, zeta, buck-boost, and sepic.

76. (Original) The output regulator of Claim 73 wherein the means for generating the sense signal is selected from a group consisting of voltage sensors, current sensors, and power sensors.

77. (Original) The output regulator of Claim 73 further including means for generating the clock signal having clock cycles; and

wherein the digital controller means to select, in synchrony with the clock signal, the one of the at least three operating modes.

78. (Original) The output regulator of Claim 77 wherein the digital controller means to switch between the at least three operating modes on a clock cycle by clock cycle basis.

79. (Original) The output regulator of Claim 74 wherein the at least three operating modes include hysteretic modes, adaptive hysteretic modes, pulse width modulated modes, constant on-time modes, constant off-time modes, resonant modes, fixed frequency soft-switching modes, voltage modes, current modes, fixed frequency modes, variable frequency modes, and combinations thereof.

80. (Original) The output regulator of Claim 78 wherein the digital controller means to generate a duty cycle estimation for controlling the generating of the power output.

81. (Original) The output regulator of Claim 80 wherein the digital controller means to generate an incremental delay to adjust the duty cycle estimation.

82. (Original) The output regulator of Claim 73 wherein the digital controller means has a switching mode selected from a group consisting of synchronous switching, asynchronous switching, and multi-frequency switching.

83. (Original) The output regulator of Claim 73 wherein the sense signal represents a difference between a reference and the regulated output.

84. (Original) The output regulator of Claim 83 wherein the reference is selected from a group consisting of reference voltages and reference currents.

85. (Original) The output regulator of Claim 73 wherein the regulated output is selected from the group comprising output voltage, output current, and output power.

86. (Original) The output regulator of Claim 73 further comprising means for output selecting to set a nominal value of the regulated output.

87. (Original) The output regulator of Claim 86 wherein the means for output selecting to generate a reference signal in response to an input, the reference signal to set the nominal value of the regulated output.